

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-7 and 19-29 are presently active in this case, Claims 8-18, previously withdrawn, are canceled and new claims 19-29 are added by the present amendment.

In the outstanding Official Action, Claims 1-7 were rejected under 35 USC 1-2(b) as anticipated by Hieda et al. (U.S. 5,998, 821, hereinafter called "Hieda").

As noted, New Claims 19-29 are submitted herewith. New Claims 19 and 28 are supported by FIG. 1. New Claims 20 and 29 are supported by FIG. 1 and the specification, at page 11, lines 4 - 8. New claim 21 is a combination of the features of Claim 1 and a further feature that a bottom surface of a gate electrode is lower than a top surface of a first conductive layer, which finds support in FIG. 1. New Claims 22-27 correspond to Claims 2-7, respectively, and find support in these original claims. No new matter has been added.

Before discussing the outstanding rejection in detail, it is believed that a brief review of the claimed invention would be helpful. In particular, in the semiconductor memory device recited in Claim 1, a top surface of a first insulation layer formed on an inner surface of a trench is located above a surface of a semiconductor substrate. As described in the specification, at page 6, line 27, "a MOS transistor T is formed on the semiconductor substrate 1 (active area)," and the surface of semiconductor 1 coincides with the interface between gate insulation layer 21 of transistor T and semiconductor 1.

Hieda discloses that SiO<sub>2</sub> film 26 is formed on the inner surface of trench 12. Unlike the claimed invention, the top surface of SiO<sub>2</sub> film 26 is not located above the surface of Si substrate 21.

The outstanding Official Action states the position that Hieda discloses the top of SiO<sub>2</sub> film 26 located above the Si substrate 21. However, Hieda, for example, as shown in FIG. 1B, shows that reference numerals 21 are given above and below buried well layer 22. From the comments presented in the Official Action, it appears that the Official Action acknowledges only a lower one of two portions having reference numerals 21 in Hieda to be a Si substrate.

However, buried well layer 22 is not formed on the surface of Si substrate 21, but within the Si substrate 21, as is clearly evident from the fact that the numerals 21 are given above and below buried well layer 22. In other words, the surface of Si substrate 21 is not the boundary between Si substrate 21 and buried well layer 22. Rather, the surface of Si substrate 21 is located in the boundary between epitaxial layer 28, which is formed on Si substrate 21, and barrier film 37.

Thus, in view of this distinction, it is respectfully submitted that the top surface of Hieda's SiO<sub>2</sub> film 26 is not located above the epitaxial layer 28 or the surface of Si substrate 21. Therefore, it is respectfully submitted that Hieda fails to disclose or obviate the structure of the claimed invention, and that the outstanding ground for rejection is traversed.

Consequently, in view of the present amendment and in light of the above comments, no further issues are believed to be outstanding, and the present application is believed to be

in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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